IN THE CLAIMS

Please cancel claims 1-10 without prejudice.

Please add claims 11-31 as follows:

WHAT IS CLAIMED IS:

1-10. (Cancelled)

11. A clock receiver circuit device comprising:

a first input adapted to be connected with a first connection of a semi-conductor component;

a second input adapted to be connected with a second connection of the semi-conductor component; and

wherein the receiver circuit device comprises more than three transfer gates.

12. The receiver circuit device according to claim 11, which comprises four transfer gates.

13. The receiver circuit device according to claim 11, comprising wherein at a first transfer gate a corresponding first transfer gate control input is connected with the second input of the receiver circuit device, and a corresponding second transfer gate control input, inverse in relation to the first transfer gate control input, is connected with the first input of the receiver circuit device.

14. The receiver circuit device according to claim 13, comprising wherein at a first transfer gate a corresponding first transfer gate control input is connected with the second input of the receiver circuit device, and a corresponding second transfer gate control input, inverse in relation to the first transfer gate control input, is connected with the first input of the receiver circuit device.

15. The receiver circuit device according to claim 14, comprising wherein at a second transfer gate connected with the first transfer gate, a corresponding first transfer gate control input is connected with the first input of the receiver circuit device, and a corresponding second transfer gate control input, inverse in relation to the first transfer gate control input is connected with the second input of the receiver circuit device.

16. The receiver circuit device according to claim 11, comprising wherein at a third transfer gate a corresponding first transfer gate control input is connected with the first input of the receiver circuit device, and a corresponding second transfer gate control input, inverse in relation to the first transfer gate control input is connected with the second input of the receiver circuit device.

17. The receiver circuit device according to claim 16, comprising wherein at a fourth transfer gate connected with third transfer gate, a corresponding first transfer gate control input is connected with the second input of the receiver circuit device, and a corresponding second transfer gate control input, inverse in relation to the first transfer gate control input, is connected with first input of the receiver circuit device.

18. The receiver circuit device according to claim 11, in which differential clock signals are present at the first and second inputs.

19. A clock receiver circuit device comprising:

a first input adapted to be connected with a first connection of a semi-conductor component;

a second input adapted to be connected with a second connection of the semi-conductor component; and

wherein the receiver circuit device comprises more than three transfer gates, and wherein a signal detectable between a first and second transfer gate and/or a second signal detectable between a third and fourth transfer gate, is used to boost a clock relaying circuit.

20. The receiver circuit device according to claim 19, comprising wherein at a first transfer gate a corresponding first transfer gate control input is connected with the second input of the receiver circuit device, and a corresponding second transfer gate control input, inverse in relation to the first transfer gate control input, is connected with the first input of the receiver circuit device.

21. The receiver circuit device according to claim 20, comprising wherein at a first transfer gate a corresponding first transfer gate control input is connected with the second input of the receiver circuit device, and a corresponding second transfer gate control input, inverse in relation to the first transfer gate control input, is connected with the first input of the receiver circuit device; and

wherein at a second transfer gate connected with the first transfer gate, a corresponding first transfer gate control input is connected with the first input of the receiver circuit device, and a corresponding second transfer gate control input, inverse in relation to the first transfer gate control input is connected with the second input of the receiver circuit device.

22. The receiver circuit device according to claim 19, comprising wherein at a third transfer gate a corresponding first transfer gate control input is connected with the first input of the receiver circuit device, and a corresponding second transfer gate control input, inverse in relation to the first transfer gate control input is connected with the second input of the receiver circuit device.

23. The receiver circuit device according to claim 22, comprising wherein at a fourth transfer gate connected with third transfer gate, a corresponding first transfer gate control input is connected with the second input of the receiver circuit device, and a corresponding second transfer gate control input, inverse in relation to the first transfer gate control input, is connected with first input of the receiver circuit device.

24. A clock receiver circuit device comprising:

a first clock input for receiving a first clock signal;

a second clock input for receiving a second clock signal, inversely equal to the first clock signal;

wherein at a first transfer gate a corresponding first transfer gate control connection is connected with the second clock input of the clock receiver circuit device, and a corresponding second transfer gate control connection, inverse in relation to the first transfer gate control connection, with the first clock input of the clock receiver circuit device; and

wherein at a second transfer gate a corresponding first transfer gate control connection is connected with the first clock input of the clock receiver circuit device, and a corresponding second transfer gate control connection, inverse in relation to the first transfer gate control connection, with the second clock input of the clock receiver circuit device,

wherein corresponding further connections of the transfer gates are connected with each other and are jointly connected with a clock output for emitting a clock output signal.

25. A semi-conductor component having a receiver comprising:

a clock receiver circuit device comprising:

a first input adapted to be connected with a first connection of a semi-conductor component;

a second input adapted to be connected with a second connection of the semi-conductor component; and

wherein the receiver circuit device comprises more than three transfer gates.

26. The component according to claim 25, wherein the receiver device circuit comprises four transfer gates.

27. The component according to claim 25, comprising wherein at a first transfer gate a corresponding first transfer gate control input is connected with the second input of the receiver circuit device, and a corresponding second transfer gate control input, inverse in relation to the first transfer gate control input, is connected with the first input of the receiver circuit device.

28. The component according to claim 27, comprising wherein at a first transfer gate a corresponding first transfer gate control input is connected with the second input of the receiver circuit device, and a corresponding second transfer gate control input, inverse in relation to the first transfer gate control input, is connected with the first input of the receiver circuit device.

29. The component according to claim 28, comprising wherein at a second transfer gate connected with the first transfer gate, a corresponding first transfer gate control input is connected with the first input of the receiver circuit device, and a corresponding second transfer gate control input, inverse in relation to the first transfer gate control input is connected with the second input of the receiver circuit device;

wherein at a third transfer gate a corresponding first transfer gate control input is connected with the first input of the receiver circuit device, and a corresponding second transfer gate control input, inverse in relation to the first transfer gate control input is connected with the second input of the receiver circuit device; and

wherein at a fourth transfer gate connected with third transfer gate, a corresponding first transfer gate control input is connected with the second input of the receiver circuit

device, and a corresponding second transfer gate control input, inverse in relation to the first transfer gate control input, is connected with first input of the receiver circuit device.

30. A clock receiver circuit device comprising:

a first clock input for receiving a first clock signal;

a second clock input for receiving a second clock signal, inversely equal to the first clock signal;

wherein at a first transfer gate a corresponding first transfer gate control connection is connected with the second clock input of the clock receiver circuit device, and a corresponding second transfer gate control connection, inverse in relation to the first transfer gate control connection, with the first clock input of the clock receiver circuit device; and

wherein at a second transfer gate a corresponding first transfer gate control connection is connected with the first clock input of the clock receiver circuit device, and a corresponding second transfer gate control connection, inverse in relation to the first transfer gate control connection, with the second clock input of the clock receiver circuit device, wherein corresponding further connections of the transfer gates are connected with each other and are jointly connected with a clock output for emitting a clock output signal.

31. A clock receiver circuit device comprising:

means for a first input adapted to be connected with a first connection of a semi-conductor component;

means for a second input adapted to be connected with a second connection of the semi-conductor component; and

wherein the receiver circuit device comprises more than three transfer gates.